Amendments to the Claims

The listing of claims will replace all prior versions and listings of claims in the application:

Listing of Claims:

1. (Canceled) An apparatus for higher radix binary multiplication, said apparatus comprising:

means for multiplying a multiplicand by weight;

means for recoding a multiplier;

means for generating partial products of low-order digits of the multiplier; and

means for combining said partial products of low-order digits of the multiplier and partial products of the multiplicand.

2. (canceled) The apparatus according to claim 1, wherein said multiplicand and multiplier are radix-32 and said multiplier is recoded to radix-7.

3. (canceled) The apparatus according to claim 1, wherein said multiplicand and multiplier are radix-256 and said multiplier is recoded to radix-11.

4. (previously presented) A method for higher radix binary multiplication, said method comprising the steps of:

receiving a multiplier and a multiplicand;

recoding the multiplier and the multiplicand by extracting bits from the multiplier and the multiplicand and obtaining first recoded digits from a conversion table;

recoding the multiplier and the multiplicand by extracting bits from the multiplier and the multiplicand and obtaining second recoded digits from a conversion table;

generating first partial products by selecting the first recoded digits in a Booth 4 partial product generator;

generating second partial products by selecting the second recoded digits in a Booth 8 partial product generator;

adding the first partial products to form a first result and multiplying the first result by 7 to form a second result;

adding the second partial products to form a third result; and

adding the second result and the third result to form a final result.

5. (previously presented) The method of claim 4, wherein the multiplier and the multiplicand are 64-bit digits and the final result is a 128-bit digit.

6. (previously presented) The method of claim 4, wherein the step of recoding to form the first recoded digits extracts 13 6-tuples of bits and the step of recoding to form the second recoded digits extracts 13 6-tuples of bits.

7. (previously presented) An apparatus for higher radix binary multiplication, said apparatus comprising:

means for receiving a multiplier and a multiplicand;

means for recoding the multiplier and the multiplicand by extracting bits from the multiplier and the multiplicand and obtaining first recoded digits from a conversion table;

means for recoding the multiplier and the multiplicand by extracting bits from the multiplier and the multiplicand and obtaining second recoded digits from a conversion table;

means for generating first partial products by selecting the first recoded digits in a Booth 4 partial product generator;

means for generating second partial products by selecting the second recoded digits in a Booth 8 partial product generator;

means for adding the first partial products to form a first result and multiplying the first result by 7 to form a second result;

means for adding the second partial products to form a third result; and

8. (previously presented) The apparatus of claim 7, wherein the multiplier and the multiplicand are 64-bit digits and the final result is a 128-bit digit.

9. (previously presented) The apparatus of claim 7, wherein the means for recoding to form the first recoded digits extracts 13 6-tuples of bits and the means for recoding to form the second recoded digits extracts 13 6-tuples of bits.

10. (previously presented) An apparatus for higher radix binary multiplication, said apparatus comprising:

a plurality of recoders;

a plurality of Booth 4 partial product generator selectors, connected to the recoders;

a plurality of Booth 8 partial product generator selectors, connected to the recoders;

an adder connected to the Booth 4 partial product generator;

an adder connected to the Booth 8 partial product generator selector;

a multiplier connected to the adder connected to the Booth 4 partial product generator; and

a carry propagate adder, connected to the adders.

11. (previously presented) A method for higher radix binary multiplication, , said method comprising the steps of:

receiving a multiplier and a multiplicand;

recoding the multiplier and the multiplicand by extracting bits from the multiplier and the multiplicand and obtaining first recoded digits from a conversion table;

recoding the multiplier and the multiplicand by extracting bits from the multiplier and the multiplicand and obtaining second recoded digits from a conversion table;

multiplying the first recoded digits of the multiplicand by 7 to form a first result; and

generating first partial products by selecting the first result in a Booth 4 partial product generator;

generating second partial products by selecting the second recoded digits in a Booth 8 partial product generator; and

adding the first partial products and the second partial products to form a final result.

12. (previously presented) The method of claim 11, wherein the multiplier and the multiplicand are 64-bit digits and the final result is a 128-bit digit.

13. (previously presented) The method of claim 11, wherein the step of recoding to form the first recoded digits extracts 13 6-tuples of bits and the step of recoding to form the second recoded digits extracts 13 6-tuples of bits.

14. (previously presented) An apparatus for higher radix binary multiplication, said apparatus comprising:

means for receiving a multiplier and a multiplicand;

means for recoding the multiplier and the multiplicand by extracting bits from the multiplier and the multiplicand and obtaining first recoded digits from a conversion table;

means for recoding the multiplier and the multiplicand by extracting bits from the multiplier and the multiplicand and obtaining second recoded digits from a conversion table;

means for multiplying the first recoded digits of the multiplicand by 7 to form a first result; and

means for generating first partial products by selecting the first result in a Booth 4 partial product generator;

means for generating second partial products by selecting the second recoded digits in a Booth 8 partial product generator; and

means for adding the first partial products and the second partial products to form a final result.

15. (previously presented) The apparatus of claim 14, wherein the multiplier and the multiplicand are 64-bit digits and the final result is a 128-bit digit.

16. (previously presented) The apparatus of claim 14, wherein the means for recoding to form the first recoded digits extracts 13 6-tuples of bits and the means for recoding to form the second recoded digits extracts 13 6-tuples of bits.

17. (previously presented) An apparatus for higher radix binary multiplication, said apparatus comprising:

a plurality of recoders;

a plurality of Booth 4 partial product generator selectors, connected to the recoders;

a plurality of Booth 8 partial product generator selectors, connected to the recoders;

a multiplier connected to the Booth 8 partial product generator selectors; and

a carry propagate adder, connected to the Booth 4 partial product generator selectors and the Booth 8 partial product generator selectors.

18. (previously presented) An apparatus for higher radix binary multiplication, said apparatus comprising:

means for receiving a multiplier and a multiplicand;

means for recoding the multiplier by extracting bits from the multiplier and obtaining first recoded digits from a first conversion table;

means for multiplying the multiplicand by 7 to form a first result;

means for generating first partial products by inputting the first result and a first recoded digit into a Booth 4 partial product generator;

means for generating second partial products by inputting the first result and respective second recoded digits into respective Booth 8 partial product generators; and

means for combining the first partial products and the second partial products to form a final result.

19. (previously presented) The apparatus of claim 18, wherein the multiplier and the multiplicand are 64-bit values and the final result is a 128-bit value.

20. (previously presented) The apparatus of claim 18, wherein the means for recoding to form the first recoded digits extracts 13 6-tuples of bits and the means for recoding to form the second recoded digits extracts 13 6-typles of bits.

21. (previously presented) An apparatus for higher radix binary multiplication, said apparatus comprising:

a plurality of recoders;

a plurality of Booth 4 partial product generator selectors, connected to the recoders;

a plurality of Booth 8 partial product generator selectors, connected to the recoders;

multiplier connected to the Booth 8 partial product generator selectors; and

a carry propagate adder, connected to the Booth 4 partial product generator selectors and the Booth 8 partial product generator selectors.